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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/789,217	02/27/2004	Chan-Yul Kim	5000-1-446	9120
33942 7590 04/20/2007 CHA & REITER, LLC 210 ROUTE 4 EAST STE 103 PARAMUS, NJ 07652			EXAMINER NGUYEN, LEON VIET Q	
			ART UNIT	PAPER NUMBER
			2611	
SHORTENED STATUTORY PERIOD OF RESPONSE		MAIL DATE	DELIVERY MODE	
3 MONTHS		04/20/2007	PAPER	

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

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<b>Office Action Summary</b>	<b>Application No.</b> 10/789,217	<b>Applicant(s)</b> KIM ET AL.	
	<b>Examiner</b> Leon-Viet Q. Nguyen	<b>Art Unit</b> 2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 27 February 2004.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2,5,10 and 11 is/are rejected.
- 7) ☒ Claim(s) 3, 4, 6-9, 12 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 27 February 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All    b) ☐ Some \*    c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Priority*

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

### ***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. **Claims 1 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Shen et al (US20020039211).**

Re claim 1, Shen discloses a clock and data recovery device capable of recovering a clock from data transmitted at a variable data rate, the CDR device comprising:

a reference clock generating section (synthesizer 1526 in fig. 5D) arranged to generate a reference clock corresponding to the variable data rate (§0078) in accordance with a control signal (synthesizer 1526 in fig. 5D controlled through communication unit 1614 by control unit 1600 in fig. 15, §0076) ;

a clock and data recovery section (CDR unit 1512 in fig. 5D) arranged to receive the transmitted data (CDR unit 1512 receiving transmitted data 160B), recover a clock and data from the received data and output the recovered clock and data (¶¶0123); and

a control section (control unit 1600 in fig. 15) arranged to generate the control signal according to the variable data rate (¶¶0076, control unit for controlling the variable rate input and output) and send the control signal to the reference clock generating section (¶¶0076, control unit 1600 in fig. 15 coupled by communication unit 1614 in fig. 5D to send signals to synthesizer 1526 in fig. 5D).

Re claim 10, Shen discloses a method for recovering a clock from data transmitted at a variable data rate, the method comprising the steps of:

generating a control signal based upon the data rate signal of a received data signal (¶¶0078);

generating a reference clock in accordance with the control signal (¶¶0078);

recovering a clock and data from the received data signal (¶¶0078); and

outputting the recovered clock and data (¶¶0123).

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

**4. Claims 2 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shen et al (US20020039211) as applied to claim 1 above, and further in view of Bellisio (US4015083).**

Re claim 2, Shen teaches a CDR device wherein said reference clock generating section (synthesizer 1526 in fig. 5D, ¶0078) comprises:

a basic clock generator arranged to generate a basic clock as an internal clock (¶0079-¶0080, the on-board reference clock interpreted to be the basic clock generator);

a first divider arranged to divide the basic clock generated by the basic clock generator by a first value P set by the control section (divider /R 1583 in fig. 5G);

a frequency detector (PFD 1585 in fig. 5G) arranged to compare the divided basic clock (the output of divider /R in fig. 5D) with an output signal;

a loop filter arranged to filter an error signal output from the frequency detector and compensate for a feedback loop (phase lock loop 1581 in fig. 5G, it is well known in the art that phase lock loops comprise of a loop filter);

a first voltage-controlled oscillator arranged to extract a phase-synchronized clock under the control of the loop filter (VCO 1591 in fig. 5G).

However Shen fails to teach wherein a CDR device comprises:

A frequency detector which compares a clock with an output signal of a multiplier and outputs an error; and

a multiplier arranged to multiply the synchronized clock output from the first voltage-controlled oscillator by a second value Q set by the control section to output the reference clock.

Bellisio teaches a timing recovery circuit (10 in fig. 1) with a frequency detector (18 in fig. 1) with multipliers (20 and 21 in fig. 1) and the timing recovery circuit outputs error signals (col. 2 lines 45-47). Bellisio also teaches a multiplier (92 in fig. 1) which multiplies the output of a controlled oscillator (22 in fig. 1) with the output of a timing extractor (15 in fig. 1, col. 2 lines 31-33, the timing extractor is interpreted to be a controller).

Therefore taking the combined teachings of Shen and Bellisio as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the timing recovery circuit of Bellisio into the CDR device of Shen. The motivation to combine Bellisio and Shen would be to reduce any differences between the bit rate of a received digital data stream and the frequency of a controlled oscillator (col. 2 lines 48-50).

Re claim 11, all of the claim limitations as recited have been analyzed and addressed in the above rejections with respect to claim 2. It would be necessary to have a method of using the apparatus as claimed in claim 2.

**5. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shen et al (US20020039211) and Bellisio (US4015083) and further in view Shimizu et al (US5524103).**

Re claim 5, the modified invention of Shen and Bellisio fails to teach a CDR device wherein the reference clock is calculated by the equation:  $f_{\text{ref}} = (\text{basic clock}) \times Q/P$  (wherein P and Q are parameters set by the control section). However Shimizu teaches a clock synthesizer (synthesizer 8 in fig. 12) which issues a reference clock (64 in fig. 12) which is calculated from a basic clock oscillator (oscillator 7 in fig. 12) divided by the frequency of a basic clock (col. 10 lines 48-51, the frequency of a basic clock is interpreted to be a control parameter).

Therefore taking the modified teachings of Shen and Bellisio with Shimizu as a whole, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the method of generating a reference clock of Shimizu into the CDR device of Shen and Bellisio. The motivation to combine Shimizu, Bellisio and Shen would be to detect errors and controlling an output such that a clock and reference clock coincide (col. 7 lines 19-23).

***Allowable Subject Matter***

**6. Claims 3, 4, 6-9, and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.**

Art Unit: 2611

**Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leon-Viet Q. Nguyen whose telephone number is 571-270-1185. The examiner can normally be reached on monday-friday, alternate friday off, 7:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Payne can be reached on 571-272-3024. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



DAVID C. PAYNE  
SUPERVISORY PATENT EXAMINER

/Leon-Viet Nguyen/